KHX4200S2LL/2G

2GB 256M x 64-Bit PC2-4200
CL3 200-Pin SODIMM

DESCRIPTION

This document describes ValueRAM's 256M x 64-bit 2GB (2048MB) PC2-4200 CL3 SDRAM (Synchronous DRAM) memory module. The module is based on sixteen 128M x 8-bit DDR2 FBGA components. The SPDs are programmed to JEDEC low latency timing of 3-3-3-8 at 1.8V. This 200-pin SODIMM uses gold contact fingers and requires +1.8V. The electrical and mechanical specifications are as follows:

SPECIFICATIONS

Clock Cycle Time (tCK) CL=3	3.7ns (min.) / 8ns (max.)
Row Cycle Time (tRC)	55ns (min.)
Refresh to Active/Refresh Command Time (tRFC)	127.5ns
Row Active Time (tRAS)	40ns (min.) / 70,000ns (max.)
Single Power Supply of	+1.8V (+/- .1V)
Power	1.396 W (operating per module)
UL Rating	94 V - 0
Operating Temperature	0° C to 55° C
Storage Temperature	-55° C to +125° C

FEATURES

- Power supply : Vdd: 1.8V ± 0.1V, Vddq: 1.8V ± 0.1V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and CK)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 5, 4, 3 (clock)
- Burst Length: 4, 8 (Interleave/nibble sequential)
- Programmable Burst type (sequential & interleave)
- Timing Reference: 3-3-3-8 at +1.8V
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : Height 1.180" (30.00mm), double sided component

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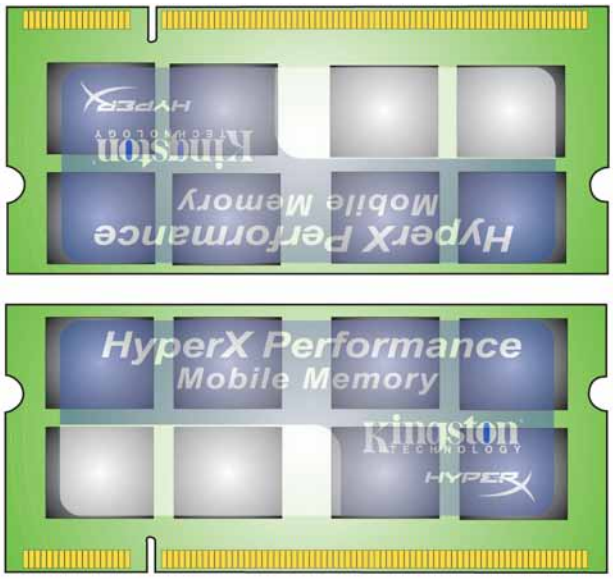
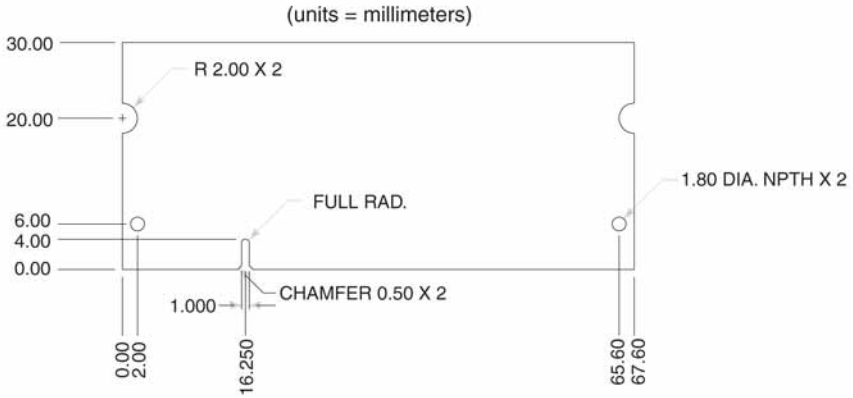
MODULE DIMENSIONS:





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