

AMD Athlon™ 64 X2

Dual-Core

Product Data Sheet



- **Compatible with Existing 32-Bit Code Base**
 - Including support for SSE, SSE2, SSE3, MMX™, 3DNow!™ technology and legacy x86 instructions
 - Runs existing operating systems and drivers
 - Local APIC on-chip
- **AMD64 Technology**
 - AMD64 technology instruction set extensions
 - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
 - Eight new 64-bit integer registers (16 total)
 - Eight new 128-bit SSE/SSE2/SSE3 registers (16 total)
- **Dual-Core Architecture**
 - Discrete L1 and L2 cache structures for each core
- **Integrated Memory Controller**
 - Low-latency, high-bandwidth
 - 128-bit DDR SDRAM at 100, 133, 166, and 200 MHz
 - Supports up to four unbuffered DIMMs
 - ECC checking with double-bit detect and single-bit correct
- **HyperTransport™ Technology to I/O Devices**
 - One 16-bit link supporting speeds up to 1 GHz (2000 MT/s) or 4 Gigabytes/s in each direction
- **64-Kbyte 2-Way Associative ECC-Protected L1 Data Caches**
 - Two 64-bit operations per cycle, 3-cycle latency
- **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Caches**
 - With advanced branch prediction
- **16-Way Associative ECC-Protected L2 Caches**
 - Exclusive cache architecture—storage in addition to L1 caches
 - Up to 1 Mbyte per L2 cache
- **Machine Check Architecture**
 - Includes hardware scrubbing of major ECC-protected arrays
- **Power Management**
 - Multiple low-power states
 - System Management Mode (SMM)
 - ACPI compliant, including support for processor performance states
- **Electrical Interfaces**
 - HyperTransport™ technology: LVDS-like differential, unidirectional
 - DDR SDRAM: SSTL_2 per JEDEC specification
 - Clock, reset, and test signals also use DDR SDRAM-like electrical specifications
- **Packaging**
 - 939 pin lidded micro PGA
 - 1.27-mm pin pitch
 - 31x31 row pin array
 - 40mm x 40mm organic substrate
 - Organic C4 die attach
- **Refer to the *AMD Functional Data Sheet, 939 Pin Package, order# 31411*, for functional, electrical, and mechanical details of 939-pin package processors.**

Publication #	33425	Revision:	3.00
Issue Date:	May 2005		

Revision History

Date	Revision	Description
May 2005	3.00	Initial public release.

Trademarks

AMD, the AMD Arrow logo, AMD Athlon, and combinations thereof, and 3DNow! are trademarks of Advanced Micro Devices, Inc.

HyperTransport is a licensed trademark of the HyperTransport Technology Consortium.

MMX is a trademark of Intel Corporation.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

Disclaimer

The contents of this document are provided in connection with Advanced Micro Devices, Inc. (“AMD”) products. AMD makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in AMD’s Standard Terms and Conditions of Sale, AMD assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

AMD’s products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of AMD’s product could create a situation where personal injury, death, or severe property or environmental damage may occur. AMD reserves the right to discontinue or make changes to its products at any time without notice.

© 2005 Advanced Micro Devices, Inc. All rights reserved.